

This listing of claims will replace all prior versions, and listings, of claims in the application.

## LISTING OF CLAIMS

1–20 (cancelled).

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21. (currently amended) A method for production of an encapsulated encapsulation for an electrical component comprising the steps of:

10       attaching a component with metallizations respectively fashioned on each of a plurality of chips a chip to a substrate in a spaced manner that has electrical connection areas so that the surface of the plurality of chips ~~chip~~ bearing component structures faces the substrate and bump connections electrically connect the metallization of the substrate with the connection areas provided on each of the plurality of chips ~~the chip~~ provide a slight distance from the  
15       substrate;

      applying a material to cover at least the lower edges of the plurality of chips ~~chip~~ and a region of the substrate abutting the edges of the plurality of chips ~~chip~~;

20       applying a first, continuous metal layer on the back side of the plurality of chips ~~chip~~, on the material and on edge regions of the substrate abutting the material; ~~and~~

      applying a second, hermetically sealing metal layer by a solvent-free process at least on the regions of the first metal layer that cover the material;

25       subsequent to applying the second metal layer on the chips, isolating the individual components by sectioning between the chips outside of the edge regions of each component;

5        wherein the step of applying the first metal layer comprises applying a  
         titanium layer and then a copper layer on each of the components,  
         the step of applying the second metal layer comprises applying a  
         metal layer selected from the group consisting of tin, tin-silver, tin-  
10       silver copper alloys and mixtures of said metals on the first metal  
         layer, said step of sectioning including removing the second metal  
         layer in the regions to be sectioned to expose the first metal layer,  
         chemically etching the exposed regions of the first metal layer to  
         remove the exposed portions and subsequently sectioning by  
15       sawing the components apart.

22. (previously presented) A method according to claim 21, wherein the step of  
applying the second metal layer provides a metal foil placed onto the first metal  
layer and includes heating to melt the metal foil onto the first metal layer.

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23. (previously presented) A method according to claim 22, wherein the step of  
providing the metal foil provides a metal foil having contours of the first metal  
layer so that it lies on the first metal layer with a positive fit.

20 24. (previously presented) A method according to claim 21, wherein the step of  
applying the second metal layer applies metal particles and then melts the  
particles onto the first metal layer.

25 25. (previously presented) A method according to claim 21, wherein the step of  
applying the second metal layer applies a metal paste and then bakes the paste  
onto the first metal layer.

26. (previously presented) A method according to claim 21, wherein the step of  
applying the second metal layer utilizes a process selected from CVD and PVD.

27. (previously presented) A method according to claim 21, wherein the step of applying a second metal layer sputters the second metal layer onto the first metal layer.

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28. (previously presented) A method according to claim 21, wherein the step of applying the second metal layer applies the second layer continuously on the first metal layer.

10 29. (previously presented) A method according to claim 21, which, after applying the first metal layer and before applying the second metal layer, includes removing surface layers of the first metal layer to improve the bonding of the second metal layer thereon.

15 30. (previously presented) A method according to claim 21, wherein, after the step of applying the first metal layer, removing an oxide layer from the first metal layer via a hydrogen plasma.

20 31. (previously presented) A method according to claim 21, wherein the step of applying the material applies a plastic film on the back side of the chip to cover the back side, the edges of the chip and subsequently seals the film with the substrate in the entire edge region around the chip.

25 32. (previously presented) A method according to claim 21, wherein the step of applying the second metal layer creates a metal alloy with a melting point greater than 260°C in the boundary surface between the first and second metal layers during the application of the second metal layer.

33. (cancelled).

34. (currently amended) A method according to claim 21 ~~33~~, wherein the step of  
5 applying the first metal layer applies a layer of titanium and a layer of copper on  
the layer of titanium.

35. (previously presented) A method according to claim 34, wherein the heating  
of the second metal layer produces a tin-copper alloy with a melting point greater  
than 260°C in the boundary between the first metal layer and the second metal  
10 layer.

36–38. (cancelled).

39. (currently amended) A method according to claim 21 ~~38~~, wherein the step of  
15 chemically etching utilizes an iron chloride solution.

40. (previously presented) A method according to claim 21, wherein the  
component is a surface wave component.